UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,939	01/16/2004	Craig Hansen	43876-153	4645

7590 04/24/2006

McDERMOTT, WILL & EMERY
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
TSAI, HENRY	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 04/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/757,939	HANSEN ET AL.	
	Examiner	Art Unit	
	Henry W.H. Tsai	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/16/04 6/10/05* .
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: *IDS: 1/31/06*.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. Claims 5 and 17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 5, it is not clear what is meant by "only one thread from the plurality of threads can handle an exception at any given time" since the exception is generally handled by the exception handler, and operating system. Similar problems exist in claim 17.

Applicant is required to review the claims and correct all language which does not comply with 35 U.S.C. § 112, second paragraph.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Ito et al. (U.S. Patent No. 5,742,782), herein referred to as Ito et al.'782.

Referring to claim 1, Ito et al.'782 discloses, as claimed, a programmable processor (see Fig. 1) comprising: a data path (comprising execution parts 25a-25d, see Fig. 1); an external interface operable to receive data from an external source (certainly existing in Ito et al.'782's system for handling input/output operation for peripherals) and communicate the received data over the data path; a register file containing a plurality of registers (register parts 26a-26c, see Fig. 1) each

having a register width (including at least 173 and 174, se Fig. 6), the register file coupled to the data path and operable to support processing of a plurality of threads (Threads A, B, and C, see Fig. 3); an execution unit (execution parts 25a-25d, see Fig. 1) coupled to the data path, the execution unit operable to execute a plurality of instruction streams from the plurality of threads (Threads A, B, and C, see Figs. 3 and Fig. 15A), each instruction stream including a single instruction that operates on a plurality of data elements (data area 173, see Fig. 6) in partitioned fields of at least one of the registers (register parts 26a-26c, see Fig. 1) to produce a catenated result, each of the data elements (data area 173, see Fig. 6) having an elemental width smaller than the register width (including at least 173 and 174, se Fig. 6). Note claims 8, 13, and 20 recite the corresponding limitations as set forth above in claim 1. Ito et al.'782 also discloses as to Claims 8 and 20 first and second registers (register parts 26a-26c, see Fig. 1).

As to claim 2, Ito et al.'782 also discloses: the processor of claim 1 wherein the execution unit (execution parts 25a-25d, see Fig. 1) comprises a pipeline (see Fig. 15B) having a plurality of stages and wherein the pipeline interleaves execution of instructions (such as A1-A12, B1-B10, and C1-C10, see Fig. 15A) from the plurality of instruction streams. Claims

9, 14, and 21, recite the corresponding limitations as set forth above in claim 2.

As to claim 3, Ito et al.'782 also discloses: the processor of claim 2 wherein the pipeline is operable to simultaneously contain states of execution of at least two instructions (such as A1-A12, B1-B10, and C1-C10, see Fig. 15A) from different instruction streams. Claims 10, 15, and 22 recite the corresponding limitations as set forth above in claim 3.

As to claim 4, Ito et al.'782 also discloses: the processor of claim 2 wherein execution of the instructions (such as A1-A12, B1-B10, and C1-C10, see Fig. 15A) is interleaved in a round-robin manner (see Fig. 15B). Claims 11, 16, and 23 recites the corresponding limitations as set forth above in claim 4.

As to claim 5, Ito et al.'782 also discloses: the processor of claim 1 wherein the processor ensures only one thread from the plurality of threads (Threads A, B, and C, see Figs. 3 and Fig. 15A) can handle an exception at any given time (see Col. 12, lines 17-23, regarding handling the exception in the Ito et al.'782's system and note one decoder (23a-23c) is handling one threat only see Fig. 1). Claim 17 recites the corresponding limitations as set forth above in claim 5.

As to claim 6, Ito et al.'782 also discloses: the processor of claim 1 further comprising a virtual memory

addressing unit and a cache operable to store data communicated between the external interface (certainly existing in Ito et al.'782's system for handling input/output operation for peripherals) and the data path. Claim 18 recites the corresponding limitations as set forth above in claim 6.

As to claim 7, Ito et al.'782 also discloses: the processor of claim 1 wherein the execution unit is further operable to, in response to decoding a second single instruction specifying a third and a fourth register (register parts 26a-26c, see Fig. 1) each containing a plurality of operands (such as source1 167 and source 2 and destination register No. 166, see Fig. 9 (a)-(c)), multiply (such as Fmult operation, see Col. 4, lines 31) the plurality of floating point operands (Fmult operation, see Col. 4, lines 31, using floating point operands) in the third register by the plurality of operands (such as source1 167 and source 2 and destination register No. 166, see Fig. 9 (a)-(c)) in the fourth register to produce a plurality of products and provide the plurality of products to partitioned fields of a result register (register parts 26a-26c, see Fig. 1) as a second catenated result. Note Claims 12, 19, and 24 recite the corresponding limitations as set forth above in claim 7.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Agarwal et al.'183 discloses a vector having a plurality of elements is stored in an input storage area, wherein the vector elements are stored in a first pattern. Thereafter, the elements are transferred, in a first order, from the input storage area into a vector register interface unit. From the vector register interface unit, the elements are transferred to an output storage area and stored in addressable locations in one of a plurality of preselected patterns.

Chung et al.'469 discloses a static interleaving technique solves the problem of resource contention in a very long instruction word multi-threaded microprocessor architecture. In the static interleaving technique, each function unit in the processor is allocated for the execution of an instruction from a particular thread in a fixed predetermined time slot in a repeating pattern of predetermined time slots.

Contact Information

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry

Tsai whose telephone number is (571) 272-4176. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Fritz M. Fleming, can be reached on (571) 272-4145. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to **the TC central telephone number, 571-272-2100.**

6. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into **the Group at fax number: 571-273-8300.** This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER

April 17, 2006